Remarks

Applicant has reviewed this Application in light of the Final Office Action dated November 17, 2008. Applicant respectfully requests reconsideration and allowance of all pending claims.

Section 112 Rejections

The Examiner rejects Claims 1-27 under 35 U.S.C. § 112, second paragraph, because the term "at least some" is allegedly not defined by the claim, the specification allegedly does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art allegedly would not be reasonably apprised of the scope of the invention.

Breadth of a claim is not to be equated with indefiniteness. *In re Miller*, 441 F.2d 689, 169 USPQ 597 (CCPA 1971). If the scope of the subject matter embraced by the claims is clear, and if applicants have not otherwise indicated that they intend the invention to be of a scope different from that defined in the claims, then the claims comply with 35 U.S.C. § 112, second paragraph. See MPEP § 2173.04. Here, Claim 1 describes collecting dynamic status information, and conveying "at least some of the dynamic status information." The claimed limitation may be broad, in that any amount of the dynamic status information may be conveyed, including all of the dynamic information, but that does not equate with indefiniteness. The element describes conveying a portion or all of the dynamic status information, and is supported by the written description. In addition, a person of ordinary skill in the art would be reasonably apprised of the scope of the claim.

The Examiner rejects Claims 25-27 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Applicant's disclosure is sufficient to convey to one skilled in the art that, as of the filing date, Applicant was in possession of the invention as claimed. In the Application, Figures 3A-3C illustrate exemplary embodiments of individual nodes 115 in grid 110. See Specification, pp. 18-24, and Figures 3A-3C. Nodes 115 may be represented by blades 314. See Specification, p. 18, lines 13-15. Blade 315 may include an integrated switch 345, which may include any number of ports. See id., p. 18, lines 26-29. Blade 315 may also include at least two processors. See id., p. 19, lines 18-21. In addition, system 100 contemplates using any suitable combination and arrangement of elements for implementing various scalability schemes. See id., p. 23, lines 23-26.

The above-cited portions of Applicant's specification, along with the rest of the Application, is sufficient to convey to one skilled in the art that, as of the filing date, Applicant was in possession of the invention as claimed. As a result, Claims 25-27 comply with the written description requirement. Consequently, Applicant respectfully requests withdrawal of the rejection of Claims 25-27.

Section 102 Rejections

The Examiner rejects Claims 1-4, 7-11, 14-18, 21, and 25-27 under 35 U.S.C. § 102(b) as being anticipated by Rena Haynes et al., *A Visual Tool for Analyzing Cluster Performance Data*, PROCEEDINGS OF THE 2001 IEEE INTERNATIONAL CONFERENCE ON CLUSTER COMPUTING, 2001 ("*Haynes*"). Applicant respectfully submits that *Haynes* fails to disclose, teach, or suggest the elements specifically recited in Applicant's claims. For example, *Haynes* fails to disclose, teach, or suggest the following elements recited in Claim 1:

> collecting dynamic status information on each of at least a subset of a plurality of nodes, each node comprising a switching fabric integrated to a card and at least two processors integrated to the card.

The Examiner points to Section 3 of *Haynes* as allegedly teaching "each node comprising a switching fabric integrated to a card and at least two processors integrated to the card." See Final Office Action, pp. 3-4. Here, *Haynes* describes a GUI that provides a visualization of network switches, where a switch may comprise twelve *processor ports*, which connect the switches to separate compute nodes, and four network ports, which connect the network switches to each other. *Haynes*, Fig. 1 and Section 3, lines 9-15 and lines 51-62 (emphasis added). The processors associated with the compute nodes that are connected to the processor ports of the switch depicted in Figure 1 may be numbered consecutively. See *Haynes*, Fig. 1 and Section 3, lines 30-32. *Haynes* therefore describes multiple processor ports in a network switch, but does not describe any configuration of the processors connected to the processor ports, including whether at least two processors are integrated to a card. *Haynes*, Section 3, lines 9-12 and 18-21. In addition, the multiple listings of "PROCESSOR" in Figure 1 denote the processor ports of a switch, not processors associated with a node. See *Haynes*, Figure 1 and Section 3. The cited portions of *Haynes* fail to describe a card and "at least two processors integrated to the card." As a result, *Haynes* fails to disclose, teach, or suggest "each node comprising a switching fabric integrated to a card and at least two processors integrated to the card" as recited in Claim 1. For at least this

reason, Claim 1 is allowable over the cited reference. Applicant respectfully requests allowance of Claim 1 and its dependents.

Similarly, Claim 8 recites "each node comprising a switching fabric integrated to a card and at least two processors integrated to the card," and Claim 15 recites "each node comprising a switching fabric integrated to a card and at least two processors integrated to the card." As discussed above with respect to Claim 1, *Haynes* fails to disclose, teach, or suggest the limitations in Claims 8 and 15. Applicant respectfully requests reconsideration and allowance of Claims 8 and 15 and their dependents.

Claim 25 recites, in part:

> at least two first processors integrated to a first card and operable to communicate with each other via a direct link between them; and
>
> a first switch integrated to the first card, the first processors communicably coupled to the first switch, the first switch operable to communicably couple the first processors to six or more second cards each comprising at least two second processors integrated to the second card and a second switch integrated to the second card operable to communicably couple the second processors to the first card and at least five third cards each comprising at least two third processors integrated to the third card and a third switch integrated to the third card[.]

The Examiner points to *Haynes*, Section 3 and Figure 1, as allegedly teaching these elements. See Final Office Action, p. 5. As discussed above with respect to Claim 1, *Haynes* merely describes a GUI that provides a visualization of network switches, where a switch may comprise twelve processor ports, which connect the switches to separate compute nodes, and four network ports, which connect the network switches to each other. *Haynes*, Fig. 1 and Section 3, lines 9-15 and lines 51-62. *Haynes* describes multiple *processor ports* in a network switch, but does not describe any configuration of the processors connected to the processor ports, including whether at least two processors are integrated to a card. *Haynes*, Section 3, lines 9-12 and 18-21. *Haynes* therefore fails to disclose, teach, or suggest "at least two first processors integrated to a first card and operable to communicate with each other via a direct link between them" as recited in Claim 25. For similar reasons, *Haynes* also fails to disclose, teach, or suggest "a first switch integrated to the first card ... and a third switch integrated to the third card" as also recited in Claim 25. For at least this reason, Claim 25 is allowable over the cited reference. Applicant respectfully requests allowance of Claim 25.

Independent Claims 26 and 27 recite elements similar to those discussed above with respect to Claim 25. For at least this reason, Claims 26 and 27 are allowable over the cited references. Applicant respectfully requests allowance of Claims 26 and 27.

Section 103 Rejections

The Examiner rejects Claims 5-6, 12-13, and 19-20 under 35 U.S.C. § 103(a) as allegedly being unpatentable over *Haynes* as applied to Claims 1-4, 8-11, and 15-18 above, and further in view of U.S. Publication No. 2003/0154112 filed by Neiman et al. ("*Neiman*"). Applicant respectfully traverses these rejections.

Claims 5-6, 12-13, and 19-20 are dependent upon independent Claims 1, 8, and 15, shown above to be allowable. For at least this reason, Claims 5-6, 12-13, and 19-20 are allowable over the cited references. Applicant respectfully requests allowance of Claims 5-6, 12-13, and 19-20 and their dependents.

Conclusion

For at least the foregoing reasons, Applicant respectfully requests allowance of all pending claims.

If a telephone conference would advance prosecution of this Application, the Examiner may call Samir A. Bhavsar, Attorney for Applicant, at 214-953-6581.

Although Applicant believes no fee is due, the Commissioner is hereby authorized to charge any fee or credit any overpayment to Deposit Account No. 02-0384 of Baker Botts L.L.P.

Respectfully submitted,

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